REMARKS

Claims 1-29 and 31-32 are pending in the present application. The rejection mailed on February 9, 2006, and the references cited therein have been considered. Favorable reconsideration is respectfully requested.

Claims 1, 2, 8, 28 and 32 were rejected under 35 U.S.C. § 102(b) as being anticipated by Martel et al (U.S. patent no. 5,887,165). Claims 1, 2, 7, 11, 19, 29 and 31 were rejected under 35 U.S.C. § 102(b) as being anticipated by O'Brien (U.S. patent no. 6,107,876). Claims 3 and 14 were rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien in view of Greif (WO 97/02570). Claims 4, 5, 9, 12, 13, 17, 18 and 25 were rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien in view of Wang (U.S. patent no. 5,765,027). Claims 10 and 15 were rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien in view of Todter et al (U.S. patent no. 5,937,070). Claim 16 was rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien in view of Keir (U.S. patent no. 5,467,400). Claims 20-22 were rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien in view of McLaughlin et al. (U.S. patent no. 3,931,474). Claims 23 and 24 were rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien in view of Ledermann (U.S. patent no. 6,278,784). Claim 27 was rejected under 35 U.S.C. § 103

as being unpatentable over O'Brien/ Greif in view of Juszkiewicz et al (U.S. patent no. 6,353,169). Claim 26 was rejected under 35 U.S.C. § 103 as being unpatentable over O'Brien/Greif in view of Suggs (U.S. patent no. 6,064,743). These rejections are respectfully traversed for the following reasons.

Claim 1 now recites a software definable pre-amplifier apparatus including an input interface means that enables at least input channel to transfer input data from an external source, and at least one reconfigurable standard cell based circuit means which are continually reconfigured during circuit operation under control of configuration data allowing the reconfigurable standard cell based circuit means to implement, in hardware, different signal processing functions required for at least one of different digital signal processing algorithms and different audio processing protocols. The reconfigurable standard cell based circuit means is reconfigured at a rate that ensures that data input from at least one of a plurality of input channels and output from at least one of a plurality of output channels is processed in accordance with the required sampling rate or sampled data rate in a way that does not cause any signal aliasing and minimizes noise artifacts on any of the operative input and output channels in relation to the selected signal

processing functions to be performed. The apparatus also includes an output interface means that transfer data from the reconfigurable standard cell based circuit means to at least one output channel, a local memory coupled to the reconfigurable standard cell based circuit means, and a host processor and associated program memory means for updating configuration data in the local memory and controlling and monitoring operation of the apparatus. The local memory stores the configuration data and is operative to supply configuration data to the reconfigurable standard cell based circuit means when a different signal processing function is to be performed.

Applicants hereby incorporate by reference the remarks made in its previous responses in the parent application.

Applicant has made a number of amendments to Claim 1 to clarify the invention:

1. Applicant has removed the term "configured in real time" as this implies Applicant's device is configured only once, when in fact it is continually reconfigured. Applicant respectfully submits that this amendment is not a narrowing amendment, because Claim 1 previously included this element.

2. In response to the Examiner's comment that "there is nothing in the claim that links the input and output channel to any specific means," Applicant has added an input interface and an output interface to show that the input and output channels are linked to a specific means. The original description mentions the input and output interfaces also shown as 2I and 2O respectively in Figure 1.

3. Applicant has replaced the term "reconfigurable circuit means" with "reconfigurable standard cell based circuit means" to indicate that Applicant is definitely not referring to FPGAs. The term "standard cell based circuit means" is used in the description (paragraph 0029 of the original) to describe a certain type of logic device.

4. Applicant has made other minor amendments to the claims, in an effort to bring them into compliance with standard U.S. practice. These amendments are not intended to change the scope of the claims.

In point 3 of the office action, the Examiner states that Martel discloses one or a plurality of reconfigurable circuit means (Fig. 1, gate array 13) which are configured in

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In point 3 of the office action, the Examiner states that Martel discloses one or a plurality of reconfigurable circuit means (Fig. 1, gate array 13) which are configured in

real time (Col. 1, lines 63-67). However, what is actually stated in Martel is: ". . . the controller to be dynamically reconfigured in real-time in response to input received from a controlled device that is linked to the controller". Also, (as mentioned in point 4 below,) the wording of col. 5, lines 4 to 14, specifically states that the gate array 13 is configured once and once only for device operation. Applicant respectfully submits that this is not performing reconfiguration during device operation to implement different algorithms or digital signal processing functions. Further, Applicant's reconfigurable standard cell based circuit means are continually reconfigured during device operation in response to implementing different digital signal processing functions/algorithms as required for a particular input/output combination. Consequently, once initiated, the continuous reconfiguration of the circuit means is autonomous. This is not the case in Martel, which requires an external controller to reconfigure the controller.

Applicant describes, in the present application, logic circuits which are continuously reconfigured, during device operation (and so these cannot be a gate array as Applicant has previously demonstrated) to implement different algorithms/functions enabling the same logic circuits to be used for different purposes.

Martel's disclosure in Fig. 1 of gate array 13, and Martel's statement in col. 1, lines 63-67, that "[t]he present invention supplies a solution to the need for allowing network-distributed real-time control and also allows the controller to be dynamically reconfigurable in real-time in response to input received from a controlled device that is linked to the controller," does not mean that the logic is continuously reconfigured during device operation to implement different functions required to implement the overall algorithm or process. The gate array 13 is only configured once in real time to implement a new standard or upgrade. This process is described in several places in Martel, for example:

> 5. The reason why gate arrays are used is to maintain compatibility with past standards and alleviate the disadvantages of dedicated equipment (Col. 1, lines 36-50). Any new configuration may take place in real time, but that could take a while to perform and is only being executed once to ensure the reconfigurable system 11 is loaded with the latest program to run. The gate array itself is then **not** being reconfigured during device operation to allow the logic to implement different functions. It

is only being reconfigured to implement a new program or standards to maintain compatibility.

6. This is further described by the wording of Col. 2, lines 52 to 57, where the description specifically states "(c) establishing the hardware configuration in the reconfigurable module." This means that the reconfigurable module is configured once and once only for operation.

7. Col. 4, lines 51 to 53 states that, "the state of the field programmable gate array remains constant as long as power is applied to the gate array's circuitry". This therefore means that the gate array is not reconfigured while running the "program" during real time device operation.

8. The wording of col. 5, lines 4 to 14, specifically states that the gate array 13 is configured once and once only for device operation. Martel states, "[p]rogramming the field programmable gate array 13 is achieved by sending the gate array a configuration signal. In response to this signal, the gate array's internal gates are set according to the contents of the configuration memory 19. After the contents of the configuration memory 19 have been

loaded, the gate array 13 now has a new hardware configuration. . . .and thereby [there is] little drain upon the host's resources,. . . ."

Those of ordinary skill in the art will recognise that the operation of the gate array as described by Martel (see points 1 - 4 above) is just the normal use of FPGAs to perform upgrades in the field and hence the reason why they are called Field Programmable Gate Arrays. It also shows why Martel's gate array is not continually being reconfigured during device operation to implement different sub-functions as described in Applicant's application. As mentioned in point 4 above, "the gate array's internal gates are set". Therefore, they cannot be being continually reconfigured during device operation.

In addition, as demonstrated in previous responses, FPGAs cannot be reconfigured many times a second as the internal circuitry does not allow this, and, more importantly, the FPGA's input/output pins are tri-stated so it cannot communicate and hence operate with external devices or perform any operations internally.

Applicant's reconfigurable logic operates in a very different manner to that of a gate array precisely to overcome the many limitations of gate arrays. Consequently, Applicant

respectfully submits that Applicant's claimed reconfigurable technology is very different to that described in Martel, and claim 1 is patentable over Martel.

With regard to point 4 of the Office Action and O'Brien, Applicant respectfully submits that the circuitry described in O'Brien specifically states that the front end 10 consists of individual circuit modules that implement specific functions, for example col. 5, line 1 (a linearizer 17), col. 5, line 13 (a noise shaper 18) and col. 5, line 30 (a pulse width modulator 19). This is also recited in claim 1 of O'Brien. However, nowhere in O'Brien is it mentioned that any of the circuitry is continuously reconfigured during device operation to implement different functions. All the circuitry is fixed to implement specific functions.

In fact, in Figure 3a, col. 6, line 65, and col. 7, line 6, O'Brien specifically mentions that more than one adder and error integrators are used. As such, these modules are therefore not reconfigured or reused. They are separate implementations of the same individual fixed circuits. This then leads to the need for more silicon real estate and a more expensive device.

The device circuitry (col. 3, lines 58 - 64) may be implemented in an ASIC, but this does not mean that the same logic circuits are continuously reconfigured during device

operation to implement different functions and there is no teaching in the O'Brien description suggesting otherwise.

The Examiner mentions "various topologies, Col. 3, lines 63-64" in relation to Applicant's different digital signal processing algorithms. What O'Brien actually states is, "of implementing various output stage topologies". In fact, in the same sentence, O'Brien specifically states, ".... that a designer using the invention is provided with flexibility in choosing the various operating parameters of the amplifier, e.g., the amplifier is capable of operating at various power levels and of implementing various output stage topologies". (Emphasis added.) Therefore, it is the designer of the amplifier who decides on the output stage topology at design and manufacture time. This is not reconfiguration and it is not logic circuits being continuously reconfigured to implement different algorithms during device operation. It is just a facility to allow designers to implement different fixed designed amplifiers.

In fact, as stated by O'Brien in col. 5, lines 46 - 55, the output stage 21 employs power switching devices and that these are preferably power MOSFET drivers. First, Applicant respectfully submits that power MOSFETs are discrete devices (effectively a single transistor) that perform a single amplification function and hence can not be

reconfigured to implement any other function. Manufacturers of these devices provide a family of devices to address the needs for implementing different power amplifiers. This is because higher spec-ed power amplifiers will need to handle higher currents and voltages and are therefore fabricated differently to handle these higher values. Applicant is submitting herewith a data sheet/power MOSFET selection guide ("Power MOFSETs progress in power switching," May 2005) to show this fact. Consequently, a designer (as stated by O'Brien) would choose the appropriate power MOSFET to suit the required output power level for a particular design. However, none of the power MOSFETs are being reconfigured.

Second, power MOSFET require different fabrication technologies to that of an ASIC and so are separate devices, especially when a high power output is required. The huge currents when compared to digital switching CMOS would require large heat sinks, as the device would operate at a very high temperature that would affect the operation of any digital circuitry.

Third, the output stage, as described in O'Brien's claim 2, can be, "any of an H bridge having totem pole outputs, a half bridge circuit, or a full bridge circuit." These are separate output topologies, but the selection of these topologies is performed by the designer at design time

as stated by O'Brien, not by any circuit means. They are also separate discrete components and are therefore not part of any ASIC device.

Also, the Examiner mentions "(i.e. various topologies, Col. 3, lines 63 - 64)" in relation to Applicant's ". . . different signal processing functions required for different digital signal processing algorithms, ..." Applicant has demonstrated above, the various topologies in O'Brien are actually various output stage topologies using discrete analog components (power MOSFETS and bridges) and these analog output stage components can not implement any of the different digital signal processing functions we describe.

Applicant is submitting herewith several commercially available data sheets showing power MOSFETs devices (power_MOSFET_device.pdf) and circuit diagrams and devices for half bridges, full bridges and H bridges (please refer to page 18 in the document H_Bridge_totem_pole.pdf, full_bridge.pdf and half_bridge.pdf). These data sheets show that these devices are analog circuits and that they are not reconfigured during device operation. The selection of any of these devices for use in the power amplifier is the choice of the designer, as stated in O'Brien, col. 3, lines 63-64.

Further, as shown in Figure 1 of O'Brien, parts of the logic circuitry (19 and 20) operate at very high

frequencies, namely 100MHz per channel. This equates to a 10 nanoseconds clock cycle time. Again, an FPGA can not be reconfigured in this short of a time period. Of course, it depends on the amount of configuration data, but tends to be in the order of milliseconds rather than nanoseconds.

For at least these reasons, Applicants respectfully submit that claim 1, as well as all the claims dependent therefrom, are patentable over O'Brien.

All of the other prior art rejections are traversed for the reason that the rejected claims depend from claim 1, and should be considered allowable along therewith.

If the above amendment should not now place the application in condition for allowance, the Examiner is invited to call undersigned counsel to resolve any remaining issues.

Respectfully submitted,

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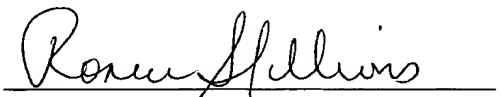
By 
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